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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/992,120	11/14/2001	Ronald Hilton	AMDH-08157US0 DEL	4631

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EXAMINER	
SAXENA, AKASH	
ART UNIT	**PAPER NUMBER**
2128	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/26/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/992,120	HILTON, RONALD	
	Examiner	Art Unit	
	Akash Saxena	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claim(s) 1-6 has/have been presented for examination based on amendment filed on 10th October 2006.
2. *Examiner would like to thank the applicant for making the response very precise and clear.*
3. No new amendments were made to the claims.
4. The arguments submitted by the applicant have been fully considered. Claims 1-6 remain rejected. The examiner's response is as follows.

Response to Applicant's Remarks on Claim Interpretation

5. Applicant has repeatedly said that his remarks were wrongly (mis)stated.

   In response to Remarks 5.1 & 5.2 applicant stated that examiner seems to miss the point that information stored in "PSW and control registers in IBM S/390 architecture" may be inaccurate at one point in time but not accurate in at a later point in time. Examiner has considered the remark however this argued limitation is not presented in the claim language. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., *spacial or temporal* accuracy of information in PSW & control register) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In response to Remarks 5.3-5.5, arguments presented are noted by examiner, that the "at a subsequent time for re-execution of translated code, there is no guarantee that the correct "program mode of operation" is stored in the "PSW and Control registers". However, the claim neither states the limitation regarding "at a subsequent time of re-execution" nor it states any limitation regarding guarantee/or lack there for values stored in "PSW and control registers".

In response to Remarks 5.6, applicant has stated that circular reasoning was presented. Examiner did not intend to present any reasoning, and merely pointing out the arguments presented in the previous remarks sent to the office (as seen under indented bullet points 2.2 and 4.2.2).

In response to Remarks 5.7, as stated earlier that, comments may be pertinent, but are not claimed. However the interpretation is noted.

Response to Applicant's Remarks for 35 U.S.C. § 102

6. Claim 1-3 and 5 were rejected under 35 U.S.C. 102(b) as being anticipated by Scalzi.

Regarding Claim 1

In Remarks 7.1, applicant states that Scalzi is limited to dynamic address translation (DAT) and computation of effective address (EA) and virtual effective address (VEA). Applicant has argued that Scalzi does not store state information with translated instructions, but rather creates an entirely new VEA address location for every different change in state information.

In response to Remarks 7.1, examiner respectfully disagrees that claimed limitation precludes teaching of Scalzi. Scalzi teaches legacy information translation is known in the art, however lack of state information (Col.4 Line 46-Col.5 Line 51) is augmented with storing the state information with the translation on per instance basis. State information is taught as "source access authorization" in this section. Examiner would further like to point out to Scalzi Col.6 Lines 22-30.

> This invention enables an *executing processor's DAT mechanism to translate a source DAT ON or OFF page* into a plurality of target virtual pages which may be translated to the same page frame in real storage. Each target virtual page is used to *represent one combinatorial set of access authorization states existing during one access of a translated page frame in real storage*. All target virtual pages translating to the same target page frame (in real storage) may herein be called "synonym" source virtual pages.

Hence Scalzi teaches the claimed limitation.

In Remarks 7.2, applicant has argued that amount of additional memory used is small compared to the operation of Scalzi. Further the present invention operates independent of whether a DAT facility is present or not whereas Scalzi is only for a DAT mechanism.

In response to Remarks 7.2, examiner asserts that it is unclaimed subject matter as to how much memory Scalzi uses or if the DAT is used or not, as these limitation are not precluded from the claimed limitations. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Further, in reference to translating source instructions and storing them, Scalzi does not limit to mapping the DAT translated pages only, as can be seen from the Scalzi (Col.6 Lines 22-25 – see above), where Scalzi handles both DAT ON and DAT OFF pages.

In Remarks 7.3-7.5, applicant has argued that Scalzi Col.6 Lines 6-59 has no discussion whatsoever of the translated instructions but only discusses addresses and DAT.

In response to Remarks 7.3-7.5, examiner agrees, however the translation is disclosed in the background of Scalzi and Scalzi (Background, Col.4 Line 46-Col.5 Line 51) whereas the cited section builds on the translated code to associate it to the state information to complete the translation, thereby curing the deficiency of the prior art.

In Remarks 7.3 & 7.6-7.7, applicant argued that there is no discussion of storing the translated instructions or storing any state information with such instructions.

In response to Remarks 7.3 & 7.6-7.7, examiner respectfully disagrees as points to Scalzi's disclosure in Background section (Scalzi Col.1-3), where various translation mechanisms like emulation, binary translation etc are disclosed to translate from one architecture to another (RISC to CISC etc). The cited section builds on the translated code to associate it to the state information to complete the translation, thereby curing the deficiency of the prior art.

Scalzi Col.7 Lines 26-31:

> It is another object of this invention to use extended (exploded) virtual effective addresses in a target machine to represent, in composite, source program access states and source program logical storage addresses for source programs designed to execute under a different computer archtitecture.

Scalzi Col.8 Line 58 -Col.9 Line 31(Subsection cited below):

> The extended target virtual addresses, in which different target addresses are used to address a single source location, one target address for each source storage access state of an access are called "exploded" target virtual addresses. This is because each source address is transformed to one of a very large number of possible target virtual addresses, depending on the state of the access control variables at the time of execution, for accesses to source machine storage as represented in the target machine storage. All accesses to source real storage made by processes of the target machine in providing source program execution are made using a target exploded effective virtual address.
>
> This invention generates a "target exploded VEA" by combining the "source EA" and the "source state indicators". The preferred combining technique is to concatenate the "source EA" and the "source state indicators" as respective fields in a target register or in real storage. Subfields in "source state indicator field" receive pre-defined source state indicator codes representing the current operating state of the access authorization mechanisms for the source program existing when the target exploded address is being generated.
>
> The target architecture may for example be the IBM PowerPC RISC architecture operating in a target microprocessor, which has a 64 bit virtual address. If the source program is using the S/390 architecture's access authorization mechanisms, the S/390 effective address requires 31 bits of the target 64 bit virtual effective address, leaving 33 bits (64-31) of the target virtual effective address for use as an appended part. Then the target virtual effective address is interpreted by the target DAT as the "exploded virtual effective address" of this invention.
>
> A major advantage of this invention using a PowerPC microprocessor (or any processor having a 64 bit virtual address) is that no modification is needed to the hardware to handle this invention, due to the availability of the 33 bits in the target virtual address (beyond the 31 bits in the source effective address) for indicating the source storage access authorization states in the exploded virtual effective address, which is then applied to the DAT feature of the microprocessor.

Although, applicant's reading of the Scalzi is correct about synonym virtual pages, the current claim does not exclude such an association/mapping. Therefore examiner respectfully disagrees that a wrongful attempt is being made to create correspondence (In response to Remarks 7.8).

Applicant's argument regarding inherency are considered and are found to be unpersuasive. Rejection is maintained.

Regarding Claim 2

Applicant has argued that (Remarks 7.10.1), no translated blocks are stored or state information associated with them. Further questions regarding block boundaries are raised. As shown before the translation whether done at execution time or before hand is associated with the state information (also see Col.7 Lines 26-31, Col.8 Line 58 -Col.10 Line 8) is stored in the virtual pages (Col.6 Lines 6-30). Applicant's arguments that no state information is stored in the blocks, is misleading in view of above teaching. Examiner respectfully maintains the rejection.

Regarding Claim 3 & 5 (Remarks 7.11 & 7.12)

Rejections are maintained for these claims in view of their dependency on rejected claim 1.

Response to Applicant's Remarks for 35 U.S.C. § 103

7. Claim(s) 6 & 8 were rejected under 35 U.S.C. 103(a) as being unpatentable over Scalzi, in view of Mann.

Regarding Claim 8 (Remarks 8.1)

Motivation to combine Mann with Scalzi is clearly defined in the rejection. The issue raised by applicant is how the DAT (disclosed by Scalzi) used with teachings of Mann. The dynamic address translation (DAT) addresses the associating the state information with the translated code, whereas dynamic object code translation (DOCT) taught by Mann is directed to instruction translation from one platform to another. Scalzi does not limit how & when the actual code is translated (one way taught by Mann) as it presents commonly known method in art in background section. Scalzi is concerned with loss of state information, which is pertinent to translated code at the time of translation. Hence, Mann performs translation of the actual code, Scalzi associates the translated code with the state information and stores it making execution of source code on the target machine possible with "source access authorization". Therefore Mann complements Scalzi in performing successful translation.

Applicant's argument regarding establishing a prima facie case of obviousness are considered and are found to be unpersuasive.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claim 1-3 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,577,231 issued to Scalzi et al (Scalzi hereafter).

Regarding Claim 1

Scalzi teaches (Original) method for dynamic emulation of legacy instructions of a legacy program (Scalzi: Col.13 Lines 26-41) by (a) providing state information for determining a program execution mode for emulating said legacy instructions (Scalzi: Col.5 Lines 18-20, Col.8 Lines 41-45) as source program containing instructions and operating states during emulation of source program; (b) accessing said legacy instructions and said state information (Scalzi: Col.8 Lines 21-40, 57-61) as current state of the executing source program representing access authorization states defined by the source architecture and for each particular legacy instruction, (c) querying to determine if one or more particular translated instructions for said execution mode are stored as a result of translating said legacy instruction for said execution mode (Scalzi: Fig.13 also see Col.9 Lines 32-62; Col.4 Line 46-Col.5 Line 51) as one or many effective translated instructions representing source instructions are translated into target instructions represented by their effective addresses, and (d) if not translated for said execution mode, translating the particular legacy

instruction into one or more particular translated instructions for emulating the particular legacy instruction for said execution mode (Scalzi: Col.4 Line 46-Col.5 Line 51; Col.6 Lines 6-59 – dynamic address translation (DAT) process checking the page table) as known process of emulation being supplemented by state information storage using the dynamic address translation, (e) *storing said one or more particular translated instructions with said state information* as storing the target address and state information associated to source code in target virtual address which is associated to translated code (Scalzi: Col.7 Lines 26-31; Col.8 Lines 58-Col.10 Lines 8), and if translated for said execution mode, continuing without additional translating (Scalzi: Col.11 Lines 12-15) as presence of valid page table entry (PTE) indicates already translated source code with state information and execution continues if valid PTE is found in the PT as detailed in Scalzi (Scalzi: Col.9 Lines 32-62), (f) accessing said one or more particular translated instructions for emulating said legacy instructions for said execution mode (Scalzi: Col.11 Lines 44-64) as source instructions along with storage authority architecture being executed on the target processor architecture.

Regarding Claim 2

Scalzi teaches storing of the one or more particular translated instructions is in one or more particular translated blocks and said state information is stored in each of said particular translated blocks as page frames (Scalzi: Col.6 Lines 6-30) as DAT based translation and exploded virtual target effective address (VEA) (Scalzi: Col.9 Lines 32-62; Col.24 Lines 55-65).

Regarding Claim 3

Scalzi teaches legacy (source) instructions are for a legacy system having a S/390 architecture (Scalzi: Col.9 Lines 13-21).

Regarding Claim 5

Scalzi teaches translated instructions are for execution in a RISC architecture (Scalzi: Col.9 Lines 13-21).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. **Claims 4 & 6 rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,577,231 issued to Scalzi et al (Scalzi hereafter), further in view of U.S. Patent No. 6516295 issued to George A. Mann et al (Mann hereafter).**

Regarding Claim 4

Teachings of Scalzi are shown in claim 1 rejection above. Scalzi is indifferent in teaching that legacy instructions are *object code instructions* compiled/assembled for a legacy architecture (Scalzi: Col.5 Lines 14-28 & Background - high level translation trivial, binary translation of object code has limited applicability). Although, his indication is clear that high-level source code translation is trivial (Col.2 Lines 1-8) and object code translation though binary translation does not reproduce access-storage-authorization mechanism - state based (Scalzi: Col.2 Lines 27-33).

Hence although not explicitly, Scalzi indirectly teaches object code based translation with accompanying state information.

Mann explicitly teaches legacy instructions are *object code instructions* compiled/assembled for a legacy architecture (Mann: Col.2 Lines 44-51).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Mann to Scalzi. Scalzi is concerned with correct state information porting while performing translation of the legacy information is major concern, source instruction code to target instruction code translation is not a specific concern which is a understood as known in art (Scalzi: Col.5 Lines 26-28). The *source instruction code to target instruction code translation* teaching is supplemented by teachings of Mann. The motivation to combine would have been that both correct state information with address translation information (taught by Scalzi) and instruction code translation (taught as DOCT by Mann Col.2 Lines 44-51) are absolutely essential for correct legacy S/390 object code to target RISC based code translation.

Regarding Claim 6

Claim 6 discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1. Preamble of claim 6 presents added limitation related to legacy code to be in object code format of the source. Mann shows this teaching in claim 4 rejection above.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 9:30 - 6:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini S. Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Friday, December 15, 2006

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